What Is Claimed Is:

1. A memory system comprising:

a memory array containing a first plurality of cells, each of first plurality of cells storing a corresponding one of a plurality of data values;

a decoding circuit selectively coupling a first cell to a bit line according to an access address, wherein said first cell is comprised in said plurality of cells; and

a sense amplifier determining whether a current path is present on said bit line, said sense amplifier generating a first logical value as an output if said current path is present on said bit line and another logical value as said output otherwise, wherein said output represents a data value stored in said first cell.

2. The memory system of claim 1, wherein said first cell is designed to provide an open path to said bit line if said another logical value is stored and a closed path to said bit line if said first logical value is stored.

3. The memory system of claim 2, wherein said sense amplifier comprises:

a first transistor having a gate terminal connected to a sense enable signal;

a second transistor and a third transistor forming a current mirror, a drain terminal of each of said second transistor and said third transistor being connected to a source terminal of said first transistor, a gate terminal of said second transistor being connected to a gate terminal of said third transistor, said gate terminal of said second transistor also being connected to a source terminal of said second transistor at a first node, said bit line also being connected to said first node;

a fourth transistor having a gate terminal connected to said sense enable signal, a drain terminal of said fourth transistor being connected to said first node;

a resistor being connected to a source terminal of said third transistor at a second node; and

an inverter having an input coupled to said second node, wherein an output of said inverter represents said output of said sense amplifier.

4. The memory system of claim 3, wherein each of said first transistor, said second transistor, and said third transistor comprises a PMOS transistor, and said fourth transistor comprises a NMOS transistor, a drain terminal of said first transistor being connected to a supply voltage, a source terminal of said fourth transistor being connected to said ground, and a second end of said resistor also being connected to said ground.

5. The memory system of claim 4 wherein each of said plurality of cells comprises a transistor, said transistor being programmed to store one logic level if said bit line is connected to a drain terminal of said transistor and another logic level otherwise.

6. The memory system of claim 5, wherein said memory array comprises a compiler memory.

7. The memory system of claim 6, wherein each of said plurality of data values comprises a bit.

8. The memory system of claim 1, wherein said memory array is provided in the form of a plurality of rows and a plurality of columns, said decoding circuit comprising:

a row decoder to select one of said plurality of rows; and

a column decoder to select one of said plurality of columns.

9. The memory system of claim 1, wherein said memory array comprises an actual memory array.

10. The memory system of claim 1, further comprising a latch coupled to said output of said sense amplifier.

11. The memory system of claim 1, wherein said sense amplifier is implemented without using a reference signal which may be used for comparison with said current to determine the value of said one of said plurality of data values to be provided on said bit line.